## **AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions and listings of claims in the application:

## LISTING OF CLAIMS:

1. (Currently Amended) A pre-decoder for a turbo decoder for decoding a turbo code consisting of a data symbol stream and a plurality of parity symbol streams, parts of which are punctured, the pre-decoder comprising:

an arithmetic unit for carrying out, a same algorithm with respect to a binary coded binary-converted data bit stream, the same algorithm that the a turbo encoder performs for generating parity bit streams, and generating an estimation value of the estimated parity bit streams;

a comparison unit for comparing non-punctured bits of [[the]] <u>binary-converted</u> parity bit streams with the <u>estimation value</u> <u>estimated parity bit streams</u> generated by the arithmetic unit;

a modulation unit for modulating the estimation value of the estimated parity bit streams generated by the calculation unit to the into estimated parity symbol streams; and

a recovery unit for recovering punctured parts of the parity symbol streams by substituting the punctured parts of the parity symbol streams for values of symbols of the estimation values corresponding to the estimated parity symbol streams for corresponding punctured parts of the parity symbol streams, when the respective related non-punctured bits of the binary-converted parity bit streams are identical with the bits of the estimation values

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corresponding bits of the estimated parity bit streams, according to a comparison result results of the comparison unit.

- 2. (Currently Amended) The pre-decoder as claimed in claim 1, wherein, when it is determined that different bits exist according to the if a comparison result of the respective non-punctured bits of the parity bit streams and the bits of the estimation values by the comparison unit indicates disagreement, the recovery unit assigns a predetermined value to a symbol of the punctured parts of the parity symbol input after a symbol corresponding to the different bits.
- 3. (Currently Amended) The pre-decoder as claimed in claim 1, wherein the arithmetic unit includes a plurality of recursive systematic convolutional (RSC) blocks corresponding to the number of the parity symbol streams, and at least one interleaver for interleaving the <u>binary-converted</u> data bit stream and providing the interleaved <u>binary-converted</u> data bit stream to at least one of the RSC blocks.
- 4. (Currently Amended) The pre-decoder as claimed in claim 1, further comprising a binary-coding binary converter unit for generating the binary-coded binary-converted data bit stream and the binary-converted parity bit streams by binary-coding binary converting the data symbol stream and the parity symbol streams, and providing the binary-coded binary-converted data bit stream and the binary-converted parity bit streams to the arithmetic unit and the comparison unit, respectively.

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- 5. (Currently Amended) The pre-decoder as claimed in claim [[1]] 4, further comprising a demultiplexer for separating the turbo code transferred output from a demodulator into the data symbol stream and the parity symbol streams and providing the data symbol stream and the parity symbol streams to the binary converter unit arithmetic unit and the comparison unit, respectively.
- 6. (Currently Amended) A method for recovering a turbo code consisting of a data symbol stream and a plurality of parity symbol streams, parts of which are punctured, the method comprising the steps of:

extracting a data symbol stream and a plurality of parity symbol streams from a received turbo code;

calculating an estimation value of estimated parity bit streams by carrying out, an algorithm with respect to a binary-converted data bit stream corresponding to the extracted data symbol stream, the same algorithm being used by a turbo encoder for producing the parity bit streams corresponding to the extracted parity symbol stream;

comparing the <u>binary-converted</u> parity <u>bit</u> <u>symbol</u> streams corresponding to the parity symbol streams with the <u>estimation value</u> <u>estimated parity bit streams</u>;

modulating the <u>estimated parity bit streams into estimated</u> <del>estimation value to the</del> parity symbol streams; and

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substituting the punctured parts of the parity symbol streams for a value of a symbol of the estimation values corresponding to the symbols of the estimated parity symbol streams for corresponding punctured parts of the parity symbol streams, when the respective related bits of the binary-converted parity bit streams are identical with the bits of the estimation values corresponding bits of the estimated parity bit streams according to a comparison result results of the comparison step.

7. (Currently Amended) The method as claimed in claim 6, further comprising a step of, in the case that different bits exist as responsive to the comparison result of non-equality in the comparison step, assigning a predetermined value to a symbol of the punctured symbols input after a symbol corresponding to the different bits.

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